SGS-THOMSON MICROELECTRONICS

QUALITY & RELIABILITY REPORT

January to December 1995 - EPROM, FLASH Memory, EEPROM and SRAM Products

INTRODUCTION

SGS-THOMSON manufactures a wide range of memory types which include:

Non-volatile memories: FLASH Memory, EPROM, OTP Memory and EEPROMs. EPROM products are manufactured in both 1.5µ NMOS and 0.8 to 0.6µ CMOS technology; FLASH Memories in 1.2 to 0.6µ CMOS technology; OTP ROMs in 0.8 to 0.6µ and EEPROMs in 1.5 to 1.0µ CMOS technology.

Packages for non-volatile memories include both ceramic FDIP and plastic PDIP, PLCC, SO and TSOP.

Static RAMs: Fast SRAM, both Synchronous and Asynchronous and NVRAMs (ZEROPOWER and TIMEKEEPER ranges). Fast SRAMs are manufactured in 0.7-0.6µ HCMOS technology; NVRAMs in 1.2-0.8µ HCMOS.

Packages for Static RAM products include the plastic PDIP, PLCC and SOJ. Some of the ZEROPOWER and TIMEKEEPER products use a modified PDIP or SO with an additional "top hat" assembly mounted above and containing a Lithium battery and optionally a quartz crystal. The battery and crystal are sealed in the plastic cap with a plastic resin.

The results presented in this quarterly report cover the tests made from January to December 1995. Regular reports are issued each quarter with the last years cumulative results.

Director of
Memory Products Group
Quality Control & Reliability

Table 1. Final Average Outgoing Quality (AOQ)

Process	Electrical ppm				Visual ppm			
	4Q95				4Q95			
UV EPROM								
CMOS	14				24			
NMOS	0				14			
OTP								
CMOS	20				8			
FLASH								
CMOS	14				5			
SRAM								
CMOS	14				3			
EEPROM								
CMOS	0				10			

Note: This data was elaborated starting from Q4/95, and will be quarterly up-dated from now on.

Table 2. Failure Rate Predictions, January to December 1995

Process	Actual Device hrs		Temperature Activation Energy (eV)	Voltage Acceleration Factor	Equivalent hrs 55 °C ($\times 10^6$)	Life Test Failure	Failure Rate (Fit) Confidence Level	
	Dev. hrs ($\times 10^6$)	Temp. (°C)					60%	90%
UV EPROM								
CMOS E5 -20%	3.73	140	0.6	4.0	1,024	0	0.9	2.2
CMOS E5 -35%	5.60	140	0.6	4.0	1,537	0	0.6	1.5
NMOS E3	5.32	140	0.6	2.6	689	0	1.3	3.3
OTP								
CMOS E5 -20%	2.27	140	0.6	4.0	589	0	1.5	3.9
CMOS E5 -35%	1.23	140	0.6	4.0	320	0	2.8	7.2
FLASH								
CMOS T4	3.92	140	0.6	3.0	763	0	1.2	3.0
CMOS T5	5.45	140	0.6	4.0	1,413	0	0.6	1.6
CMOS T5 -20%	6.56	140	0.6	4.0	1,700	0	0.5	1.3
SRAM								
CMOS Spectrum	0.38	125	0.7	64	1,897	0	0.5	1.2
HCMOS S3	0.30	125	0.7	64	1,498	0	0.6	1.5
HCMOS 4P	2.68	125	0.7	5.7	1,175	7	7.1	10
HCMOS 4PS	2.10	125	0.7	13	2,058	6	3.6	5.1
HCMOS 4PL	1.106	125	0.7	58	4,939	1	0.4	0.8
EEPROM								
CMOS F4	2.62	140	0.6	3.0	616	0	1.4	3.7

Table 3. NMOS E3/1.5µm Process UV EPROM Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M2716		M2732A		M2764A		M27128A		M27256		M27512	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	272	0	164	0	15,586	0	8,790	0	7,730	0	3,690	0
		– 168 hrs	272	0	164	0	2,133	0	1,404	0	702	0	2,229	0
		– 500 hrs	272	0	164	0	1,418	0	234	0	668	0	1,080	0
		– 1000 hrs	272	0	164	0	1,218	0	117	0	234	0	963	0
Retention Bake	1008	250°C,												
		– 48 hrs	250	0	175	0	1,300	0	400	0	600	0	900	0
		– 168 hrs	250	0	175	0	1,300	0	400	0	600	0	900	0
		– 500 hrs	250	0	175	0	1,300	0	400	0	500	0	900	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 4. CMOS E5/0.8µm Process UV EPROM Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C64A	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,		
		– 48 hrs	1,928	0
		– 168 hrs	234	0
		– 500 hrs	234	0
		– 1000 hrs	234	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C,		
		– 48 hrs	200	0
		– 168 hrs	200	0
		– 500 hrs	200	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 5. CMOS E5/0.8µm Process (–10% upgrade) UV EPROM Reliability Data, Die Related Tests, January to December1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B (B) M87C257	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz, (50% '0')		
		– 48 hrs	12,777	0
		– 168 hrs	135	0
		– 500 hrs	135	0
		– 1000 hrs	135	0
		– 2000 hrs	-	-
Retention Bake	1008	250°C, (99% '0')		
		– 48 hrs	200	0
		– 168 hrs	200	0
		– 500 hrs	200	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 6. CMOS E5/0.8µm Process (-20% upgrade) UV EPROM Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512 (C)		M27C1001 (C)		M27C1024 (B)		M27C2001 (C)		M27C4001 (D)		M27C4002 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,												
		– 48 hrs	12,700	0	882	0	2,128	0	1,124	0	435	0	8,824	0
		– 168 hrs	1,143	0	805	0	200	0	200	0	135	0	123	0
		– 500 hrs	1,143	0	805	0	200	0	200	0	135	0	123	0
		– 1000 hrs	1,143	0	805	0	200	0	200	0	135	0	123	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Retention Bake	1008	250°C,												
		– 48 hrs	900	0	296	0	200	0	50	0	200	0	50	0
		– 168 hrs	900	0	296	0	200	0	50	0	200	0	50	0
		– 500 hrs	900	0	296	0	200	0	50	0	200	0	50	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-	-	-

Notes: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 7. CMOS E5/0.8µm Process (-35% upgrade) UV EPROM Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)		M27C801		M27C160	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz,										
		– 48 hrs	15,047	0	6,991	0	11,010	0	9,741	0	3,363	0
		– 168 hrs	3,579	0	200	0	3,541	0	266	0	283	0
		– 500 hrs	777	0	200	0	1,219	0	266	0	283	0
		– 1000 hrs	543	0	200	0	1,102	0	266	0	283	0
		– 2000 hrs	96	0	144	0	96	0	-	-	-	-
Retention Bake	1008	250°C,										
		– 48 hrs	1,500	0	200	0	1,696	0	150	0	150	0
		– 168 hrs	1,500	0	200	0	1,696	0	150	0	150	0
		– 500 hrs	1,500	0	200	0	1,696	0	150	0	150	0
		– 1000 hrs	-	-	-	-	-	-	-	-	-	-

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 8. UV EPROM Reliability Data, Package Related Tests (Ceramic Frit-Seal), January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 500 cycles – 1000 cycles	 3,350 3,350 2,050	 0 0 0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Thermal Shock	1011	–55 to 125°C, – 60 cycles	275	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Salt Atmosphere	1009	Test Condition A, 35°C	25	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Solderability	2003	245°C, 5sec, Precondition Steam, 1hr	1,235	0
Resistance to Solvents	2015	4 Solvent Solutions	260	0
Lead Integrity	2004	Test Condition B2 (lead fatigue)	225	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Test Procedure	MIL-STD-883 Procedure	Test Conditions	Samp.	Fail
Environmental Sequence:				
1. Thermal Shock	1011	–55 to 125°C, 15 cycles		
2. Temperature Cycling	1010	–65 to 150°C, 100 cycles	50	0
3. Moisture Resistance	1004	–10 to 65°C, RH = 90%, 10 cycles of 24hrs		
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Mechanical Sequence:				
1. Mechanical Shock	2002	Test Condition B		
2. Vibration Variable Frequency	2007	Test Condition A	50	0
3. Constant Acceleration	2001	Test Condition E		
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		
Temperature Cycling	1010	–65 to 150°C, 10 cycles		
Constant Acceleration	2001	Test Condition E	50	0
– Fine Leak – Gross Leak	1014 1014	Test Condition A1 Test Condition C1		

Table 9. CMOS E5/0.8µm Process (–10% Upgrade) OTP Memory Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B M87C257	
			Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz		
		– 168 hrs	816	0
		– 500 hrs	816	0
		– 1000 hrs	768	0
		– 2000 hrs	288	0
Retention Bake	1008	150°C,		
		– 168 hrs	975	0
		– 500 hrs	975	0
		– 1000 hrs	975	0
		– 2000 hrs	217	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 10. CMOS E5/0.8µm Process (–10% Upgrade) OTP Memory Reliability Data, Package Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C256B M87C257	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,		
		– 168 hrs	650	0
		– 500 hrs	650	0
		– 1000 hrs	550	0
		– 2000 hrs	248	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,		
		– 48 hrs	503	0
		– 96 hrs	503	0
		– 168 hrs	503	0
		– 240 hrs	195	0
Pressure Pot		121°C, 2Atm,		
		– 48 hrs	960	0
		– 96 hrs	960	0
		– 168 hrs	960	0
		– 240 hrs	960	0
Temperature Cycling	1010	–65 to 150°C,		
		– 100 cycles	1,080	0
		– 500 cycles	1,080	0
		– 1000 cycles	1,080	0
Solderability:				
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	150	0
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	50	0
Resistance to Solvents	2015	4 Solvent Solutions	120	0

Table 11. CMOS E5/0.8µm Process (–20% Upgrade) OTP Memory Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512		M27C1001		M27C1024		M27C2001		M27C4001		M27C4002	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz												
		– 168 hrs	480	0	282	0	432	0	223	0	385	0	477	0
		– 500 hrs	480	0	282	0	336	0	223	0	385	0	477	0
		– 1000 hrs	384	0	282	0	96	0	223	0	385	0	384	0
		– 2000 hrs	96	0	48	0	-	-	-	-	48	0	96	0
Retention Bake	1008	150°C,												
		– 168 hrs	660	0	240	0	410	0	100	0	120	0	590	0
		– 500 hrs	660	0	240	0	410	0	100	0	120	0	590	0
		– 1000 hrs	660	0	240	0	410	0	100	0	120	0	590	0
		– 2000 hrs	180	0	-	-	180	0	-	-	60	0	230	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 12. CMOS E5/0.8µm Process (–20% Upgrade) OTP Memory Reliability Data, Package Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C512		M27C1001		M27C1024		M27C2001		M27C4001		M27C4002	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,												
		– 168 hrs	550	0	200	0	460	0	45	0	100	0	400	0
		– 500 hrs	550	0	200	0	460	0	45	0	100	0	400	0
		– 1000 hrs	450	0	200	0	460	0	45	0	100	0	400	0
		– 2000 hrs	100	0	50	0	50	0	-	-	-	-	100	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,												
		– 48 hrs	250	0	56	0	280	0	28	0	56	0	252	0
		– 96 hrs	250	0	56	0	280	0	28	0	56	0	252	0
		– 168 hrs	250	0	56	0	252	0	28	0	56	0	252	0
		– 240 hrs	111	0	-	-	84	0	-	-	28	0	56	0
Pressure Pot		121°C, 2Atm,												
		– 48 hrs	800	0	180	0	471	0	50	0	120	0	536	0
		– 96 hrs	800	0	180	0	471	0	50	0	120	0	536	0
		– 168 hrs	800	0	180	0	471	0	50	0	120	0	536	0
		– 240 hrs	800	0	180	0	471	0	50	0	60	0	480	0
Temperature Cycling	1010	–65 to 150°C,												
		– 100 cycles	540	0	240	0	540	0	25	0	120	0	600	0
		– 500 cycles	540	0	240	0	540	0	25	0	120	0	600	0
		– 1000 cycles	540	0	240	0	540	0	25	0	120	0	600	0
Solderability:														
– PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 320/0											
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 70/0											
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 288/0											

Table 13. CMOS E5/0.8µm Process (–35% Upgrade) OTP Memory Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V, f = 500kHz						
		– 168 hrs	339	0	373	0	426	0
		– 500 hrs	339	0	373	0	426	0
		– 1000 hrs	339	0	373	0	426	0
		– 2000 hrs	48	0	-	-	48	0
Retention Bake	1008	150°C,						
		– 168 hrs	300	0	150	0	540	0
		– 500 hrs	300	0	150	0	540	0
		– 1000 hrs	300	0	150	0	540	0
		– 2000 hrs	60	0	-	-	120	0

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 14. CMOS E5/0.8µm Process (–35% Upgrade) OTP Memory Reliability Data, Package Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M27C1001 (E)		M27C2001 (E)		M27C4001 (E)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	250	0	200	0	300	0
		– 500 hrs	250	0	200	0	300	0
		– 1000 hrs	250	0	200	0	300	0
		– 2000 hrs	50	0	50	0	50	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	194	0	28	0	306	0
		– 96 hrs	194	0	28	0	306	0
		– 168 hrs	167	0	28	0	252	0
		– 240 hrs	56	0	28	0	56	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	300	0	270	0	360	0
		– 96 hrs	300	0	270	0	360	0
		– 168 hrs	300	0	270	0	360	0
		– 240 hrs	300	0	270	0	360	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	360	0	240	0	420	0
		– 500 cycles	360	0	240	0	420	0
		– 1000 cycles	360	0	240	0	360	0
Solderability:								
– PLCC/TSOP Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 395/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 125/0					
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 208/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 15. CMOS T4/1.2µm Process FLASH Memory Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 - M28F256A		M28F512	
			Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 24 hrs	36,802	0	69,493	0
		– 168 hrs	432	0	508	0
		– 500 hrs	432	0	508	0
		– 1000 hrs	432	0	508	0
		– 2000 hrs	240	0	220	0
Retention Bake (1)	1008	150°C,				
		– 168 hrs	448	0	952	0
		– 500 hrs	448	0	952	0
		– 1000 hrs	448	0	952	0
		– 2000 hrs	150	0	360	0
Write/Erase Cycling		1,000 cycles	4,832	0	14,261	1 (a)
		10,000 cycles	-	-	614	1 (b)
Retention Bake	1008	150°C, 36 hrs	4,832	0	14,261	0

Notes: 1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
Fail a. Programming Failure, single bit failures.
Fail b. Erasing Failure, single bit failures.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 16. CMOS T4/1.2µm Process FLASH Memory Reliability Data, Package Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 - M28F256A		M28F512	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	598	0	460	0
		– 500 hrs	598	0	460	0
		– 1000 hrs	598	0	460	0
		– 2000 hrs	150	0	210	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 48 hrs	166	0	189	0
		– 96 hrs	166	0	189	0
		– 168 hrs	166	0	189	0
		– 240 hrs	56	0	53	0
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	440	0	400	0
		– 96 hrs	440	0	400	0
		– 168 hrs	440	0	400	0
		– 240 hrs	440	0	400	0
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	390	0	320	0
		– 500 cycles	390	0	320	0
		– 1000 cycles	360	0	320	0
Thermal Shock	1011	–55 to 125°C,				
		– 100 cycles	25	0	25	0
		– 500 cycles	25	0	25	0
Solderability:						
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 305/0			
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 50/0			
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 284/0			

Table 17. CMOS T5/0.8µm Process FLASH Memory Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F101		M28F102	
			Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V, f = 500kHz,				
		– 24 hrs	85,292	0	88,594	0
		– 168 hrs	768	0	192	0
		– 500 hrs	768	0	144	0
		– 1000 hrs	768	0	144	0
		– 2000 hrs	336	0	48	0
Retention Bake (1)	1008	150°C,				
		– 168 hrs	798	0	310	0
		– 500 hrs	798	0	310	0
		– 1000 hrs	798	0	310	0
		– 2000 hrs	400	0	100	0
Retention Bake	1008	250°C,				
		– 168 hrs	146	0	-	-
		– 500 hrs	146	0	-	-
		– 1000 hrs	146	0	-	-
		– 2000 hrs	146	0	-	-
Write/Erase Cycling		1,000 cycles	15,475	3 (a)	15,808	0
		10,000 cycles	472	2 (b)	81	0
Retention Bake	1008	150°C, 36 hrs	15,475	0	15,808	0

Notes: 1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
Fail a. Programming Failure, single bit failure.
Fail b. Erasing Failure, single bit failure.

Table 18. CMOS T5/0.8µm Process FLASH Memory Reliability Data, Package Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F101		M28F102	
			Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,				
		– 168 hrs	400	0	200	0
		– 500 hrs	400	0	200	0
		– 1000 hrs	400	0	100	0
		– 2000 hrs	100	0	100	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,				
		– 48 hrs	250	0	137	0
		– 96 hrs	250	0	137	0
		– 168 hrs	250	0	137	0
		– 240 hrs	56	0	110	0
Pressure Pot		121°C, 2Atm,				
		– 48 hrs	400	0	200	0
		– 96 hrs	400	0	200	0
		– 168 hrs	400	0	200	0
		– 240 hrs	400	0	200	0
Temperature Cycling	1010	–65 to 150°C,				
		– 100 cycles	420	0	150	0
		– 500 cycles	420	0	150	0
		– 1000 cycles	420	0	150	0
Thermal Shock	1011	–55 to 125°C,				
		– 100 cycles	25	0	25	0
		– 500 cycles	25	0	25	0
Solderability:						
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 405/0			
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 213/0			
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 276/0			

Table 19. CMOS T5/0.8µm Process (–20% upgrade) FLASH Memory Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test (1)	1005	140°C, V_{CC} = 6V, f = 500kHz,						
		– 24 hrs	6,076	0	4,233	0	175,953	0
		– 168 hrs	76	0	246	0	1,301	0
		– 500 hrs	76	0	246	0	1,253	0
		– 1000 hrs	76	0	246	0	1,059	0
		– 2000 hrs	76	0	195	0	372	0
Retention Bake (1)	1008	150°C,						
		– 168 hrs	50	0	100	0	1,308	0
		– 500 hrs	50	0	100	0	1,308	0
		– 1000 hrs	50	0	100	0	1,058	0
		– 2000 hrs	50	0	100	0	513	0
Retention Bake	1008	250°C,						
		– 168 hrs	-	-	-	-	1,435	0
		– 500 hrs	-	-	-	-	1,435	0
		– 1000 hrs	-	-	-	-	1,435	0
		– 2000 hrs	-	-	-	-	1,223	0
Write/Erase Cycling		1,000 cycles	1,181	0	877	0	19,826	3 (a)
		10,000 cycles	-	-	-	-	282	1 (b)
Retention Bake	1008	150°C, 36 hrs	1,181	0	877	0	19,826	0

Notes: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.
1. A quarter of sample size was subjected to 10,000 Write/Erase cycles before operating life test and retention bake.
Fail a. Programming Failure, single bit failure.
Fail b. Erasing Failure, single bit failure.

Table 20. CMOS T5/0.8µm Process (–20% upgrade) FLASH Memory Reliability Data, Package Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28F256 (B)		M28F512 (B)		M28F101 (B)	
			Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,						
		– 168 hrs	48	0	96	0	670	0
		– 500 hrs	48	0	96	0	670	0
		– 1000 hrs	48	0	96	0	520	0
		– 2000 hrs	48	0	96	0	270	0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V,						
		– 48 hrs	44	0	88	0	322	0
		– 96 hrs	44	0	88	0	322	0
		– 168 hrs	44	0	88	0	322	0
		– 240 hrs	44	0	88	0	159	0
Pressure Pot		121°C, 2Atm,						
		– 48 hrs	120	0	200	0	690	0
		– 96 hrs	120	0	200	0	690	0
		– 168 hrs	120	0	200	0	690	0
		– 240 hrs	120	0	200	0	570	0
Temperature Cycling	1010	–65 to 150°C,						
		– 100 cycles	96	0	128	0	740	0
		– 500 cycles	96	0	128	0	740	0
		– 1000 cycles	96	0	128	0	680	0
Thermal Shock	1011	–55 to 125°C,						
		– 100 cycles	-	-	-	-	100	0
		– 500 cycles	-	-	-	-	75	0
Solderability:								
– TSOP, PLCC Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 290/0					
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 100/0					
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 172/0					

Note: In the Part Number, the letter in brackets represents the Die revision identifier. This letter is marked after the datecode on device marking.

Table 21A. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01C ST24W01C		ST24C02C ST24W02C		ST24C04C ST24W04C		ST24C16C ST24W16 ST24E16D ST24164	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,								
		– 24 hrs	250	0	10,200	0	2,550	0	-	-
		– 168 hrs	250	0	2,200	0	550	0	-	-
		– 500 hrs	250	0	2,200	0	550	0	-	-
		– 1000 hrs	-	-	-	-	-	-	-	-
Retention Bake	1008	150°C,								
		– 168 hrs	50	0	1,200	0	450	0	100	0
		– 500 hrs	50	0	1,200	0	450	0	100	0
		– 1000 hrs	50	0	1,200	0	450	0	100	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	-	-	950	0	500	0	50	0
		1,000,000 cycles	-	-	950	0	500	0	50	0
Retention Bake	1008	150°C, 168 hrs	-	-	950	0	500	0	50	0

Table 21B. CMOS F4/1.2µm Process EEPROM Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M28C64C		ST93C06C ST93C46C	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,				
		– 24 hrs	78	0	11,200	0
		– 168 hrs	78	0	1,200	0
		– 500 hrs	78	0	1,200	0
		– 1000 hrs	-	-	-	-
Retention Bake	1008	150°C,				
		– 168 hrs	300	0	800	0
		– 500 hrs	300	0	800	0
		– 1000 hrs	200	0	800	0
		– 2000 hrs	-	-	-	-
Write/Erase Cycling		100,000 cycles	400	0	1,200	0
		1,000,000 cycles	-	-	1,100	0
Retention Bake	1008	150°C, 168 hrs	400	0	1,200	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 22. CMOS F4/1.2µm Process EEPROM Reliability Data, Package Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01C ST24W01C		ST24C02C ST24W02C		ST24C04C ST24W04C		ST24C16C ST24W16 ST24E16D ST24164		M28C64C		ST93C06C ST93C46C	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,												
		– 168 hrs	60	0	1,050	0	180	0	300	0	478	0	720	0
		– 500 hrs	60	0	1,050	0	180	0	300	0	478	0	720	0
		– 1000 hrs	60	0	1,050	0	180	0	300	0	478	0	720	0
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,												
		– 48 hrs	100	0	1,750	0	400	0	900	0	450	0	750	0
		– 96 hrs	100	0	1,750	0	400	0	900	0	450	0	750	0
		– 168 hrs	100	0	1,750	0	400	0	900	0	450	0	750	0
		– 240 hrs	100	0	1,750	0	400	0	900	0	450	0	750	0
Temperature Cycling	1010	–65 to 150°C,												
		– 100 cycles	100	0	1,750	0	400	0	900	0	450	0	750	0
		– 200 cycles	-	-	-	-	-	-	-	-	-	-	-	-
		–40 to 150°C,												
		– 500 cycles	-	-	-	-	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-	-	-	-	-
Solderability:														
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 588/0											
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 512/0											
– PLCC Package			Cumulative Sample/Fail = 25/0											
– TSOP Package			Cumulative Sample/Fail = 25/0											
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 136/0											
Resististance to Surface Mount:														
– SO Package			Cumulative Sample/Fail = 900/0											
– TSOP Package			Cumulative Sample/Fail = -/-											

Table 23. CMOS F4S/1.0µm Process EEPROM Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24C08		ST24LC21	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Operating Life Test	1005	140°C, V_{CC} = 6V,										
		– 168 hrs	350	0	550	0	100	0	224	0	72	0
		– 500 hrs	350	0	550	0	100	0	224	0	72	0
		– 1000 hrs	-	-	-	-	49	0	224	0	-	-
Retention Bake	1008	150°C,										
		– 168 hrs	100	0	150	0	-	-	-	-	60	0
		– 500 hrs	100	0	150	0	-	-	-	-	60	0
		– 1000 hrs	100	0	150	0	-	-	-	-	-	-
		– 2000 hrs	-	-	-	-	-	-	-	-	-	-
Write/Erase Cycling		100,000 cycles	150	0	300	0	100	0	-	-	58	0
		1,000,000 cycles	100	0	300	0	100	0	-	-	58	0
Retention Bake	1008	150°C, 168 hrs	150	0	300	0	100	0	-	-	58	0

Table 24. CMOS F4S/1.0µm Process EEPROM Reliability Data, Package Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	ST24C01 ST24W01		ST24C02 ST24W02		ST24C04 ST24W04		ST24E32	
			Samp.	Fail	Samp.	Fail	Samp.	Fail	Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V,								
		– 168 hrs	120	0	120	0	-	-	80	0
		– 500 hrs	120	0	120	0	-	-	80	0
		– 1000 hrs	120	0	120	0	-	-	80	0
		– 2000 hrs	-	-	-	-	-	-	-	-
Pressure Pot		121°C, 2Atm,								
		– 48 hrs	150	0	450	0	100	0	400	0
		– 96 hrs	150	0	450	0	100	0	400	0
		– 168 hrs	150	0	450	0	100	0	400	0
		– 240 hrs	150	0	450	0	100	0	400	0
Temperature Cycling	1010	–65 to 150°C,								
		– 100 cycles	150	0	450	0	50	0	300	0
		– 200 cycles	-	-	-	-	-	-	-	-
		–40 to 150°C,								
		– 500 cycles	-	-	-	-	-	-	-	-
		– 1000 cycles	-	-	-	-	-	-	-	-
Solderability:										
– PDIP Package	2003	245°C, 5sec, Precondition Steam, 8hr	Cumulative Sample/Fail = 24/0							
– SO Package	CECC 90,000	215°C, 3sec, Precondition Dry Air, 150°C, 16hr	Cumulative Sample/Fail = 168/0							
– PLCC Package			Cumulative Sample/Fail = -/-							
– TSOP Package			Cumulative Sample/Fail = -/-							
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = 120/0							
Resististance to Surface Mount:										
– SO Package			Cumulative Sample/Fail = 200/0							
– TSOP Package			Cumulative Sample/Fail = -/-							

Table 25. CMOS SPECTRUM/2.0μm Process ZEROPOWER SRAM Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f =1MHz		
		– 168 hrs	385	0
		– 500 hrs	385	0
		– 1000 hrs	385	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 26. CMOS SPECTRUM/2.0µm Process ZEROPOWER SRAM Reliability Data, Package Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T02	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 385 385 385	 0 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles	 385 385	 0 0
Resistance to Solvents	2015	4 Solvent Solutions	60	0

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 27. HCMOS S3/1.2µm Process ZEROPOWER SRAM Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 7V, f =1KHz		
		– 168 hrs	304	0
		– 500 hrs	304	0
		– 1000 hrs	304	0

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 28. HCMOS S3/1.2µm Process ZEROPOWER SRAM Reliability Data, Package Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	MK48T08	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 181 181 181	 0 0 0
Temperature Cycling SOIC	1010	–65 to 150°C, – 100 cycles – 300 cycles – 600 cycles – 1000 cycles	 75 75 75 75	 0 0 0 0
Temperature Cycling CAPHAT	1010	–40 to 125°C, – 100 cycles – 300 cycles – 600 cycles – 1000 cycles	 126 116 65 65	 0 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 168 hrs	 - -	 - -
Resistance to Solvents	2015	4 Solvent Solutions	24	0

Table 29. HCMOS 4P/0.7µm Process SRAM Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628128 M624256	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1MHz		
		– 168 hrs	3,924	3 (a)
		– 500 hrs	1,740	2 (a)
		– 1000 hrs	1,153	2 (a)
		– 2000 hrs	865	0

Note: Fail a. All failures are due to single bits and are suspected to be related to particles as shown from past failure analysis results of similar type failures.

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 30. HCMOS 4P/0.7µm Process SRAM Reliability Data, Package Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628128 M624256	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 422 200 77	 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 192 hrs	 145 145	 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles – 600 cycles – 1000 cycles	 580 530 333 235	 0 0 0 0
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-	

Operating Life Test

Aim:To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 31. HCMOS 4PS/0.6µm Process SRAM Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M624256 M628128		M628032	
			Samp.	Fail	Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 6V, f =1MHz				
		– 168 hrs	1,730	2 (a)	247	1 (d)
		– 500 hrs	1,176	1 (b)	247	1 (e)
		– 1000 hrs	1,175	0	77	0
		– 2000 hrs	597	1 (c)	77	0

Notes: Multiple process improvements have been implemented to address polysilicon particle reduction, and have been verified to reduce defects.
Fail a. 1 oxide particle between M1 and M2.
1 single bit, no defect found.
Fail b. Single bit failure due to particle between poly 2 and poly 3.
Fail c. Single bit, no defect found.
Fail d. Single bit failure due to particle at poly 2.
Fail e. I_{CC3} failure at 70°C.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 32. HCMOS 4PS/0.6µm Process SRAM Reliability Data, Package Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M628032	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 5V, – 168 hrs – 500 hrs – 1000 hrs	 127 127 127	 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 5V, – 96 hrs – 192 hrs	 42 42	 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles – 600 cycles – 1000 cycles	 213 213 213 213	 0 0 0 0
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-	

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 33. HCMOS 4PL/0.5µm 3.3V Process SRAM Reliability Data, Die Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M638032	
			Samp.	Fail
Operating Life Test	1005	125°C, V_{CC} = 4.2V, f =1MHz		
		– 168 hrs	1,834	1 (a)
		– 500 hrs	599	0
		– 1000 hrs	599	0
		– 1500 hrs	599	0

Notes: Fail a. Single bit failure at 48 hrs due to scratch causing Si damage in the gate.

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 34. HCMOS 4PL/0.5µm 3.3V Process SRAM Reliability Data, Package Related Tests, January to December 1995

Test Procedure	MIL-STD-883 Procedure	Test Conditions	M638032	
			Samp.	Fail
Temperature, Humidity, Bias	CECC 90,000	85°C, RH = 85%, V_{CC} = 3.3V, – 168 hrs – 500 hrs – 1000 hrs – 2000 hrs	 171 171 171 171	 0 0 0 0
HAST	CECC 90,000	130°C, RH = 85%, V_{CC} = 3.3V, – 96 hrs – 192 hrs	 142 142	 0 0
Temperature Cycling	1010	–65 to 150°C, – 100 cycles – 300 cycles – 600 cycles – 1000 cycles	 231 231 231 231	 0 0 0 0
Resistance to Solvents	2015	4 Solvent Solutions	Cumulative Sample/Fail = -/-	

Operating Life Test

Aim: To predict the device resistance to operating electrical stress, accelerated by temperature over a short and long term.

Detects Failure Mechanisms Originating from:

- Electromigration in metal connections
- Contact spiking
- Process contamination
- Oxides defects
- Misplaced or weakened wire bonds
- Damaged wires
- Device surface damage

Table 35. Statistical Process Control: NMOS E3/1.5µm Process UV EPROM, Rousset - France Diffusion Line

Key Process Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Gate Oxide Thickness	1.34	1.29	1.25	1.04	2.38	2.22	1.41	1.22
Interpoly Oxide Thickness (1)	2.05	1.11	1.53	1.45	2.06	1.80	1.08	1.06
Field Oxide Thickness	1.78	1.59	1.68	1.52	2.48	2.46	1.84	1.82
Intermediate Dielectric Thickness	4.52	4.40	7.28	7.02	5.31	5.11	3.01	2.76
Final P-Vapox Thickness	6.06	4.90	3.99	3.76	4.30	4.23	4.61	4.15
Polysilicon I Thickness	2.82	2.77	1.43	1.39	1.97	1.71	2.19	2.10
Polysilicon II Thickness	2.47	2.36	1.89	1.82	2.30	2.12	2.53	2.42
Aluminium 1% Si Thickness (SP1)	2.31	2.18	2.09	1.97	2.95	2.74	2.45	2.35
Polysilicon II Critical Dimensions	1.88	1.55	2.20	1.80	2.21	1.91	1.53	1.45
Active Area Critical Dimensions	3.67	3.13	1.44	1.36	3.18	3.13	2.61	2.15

Note: 1. To redefine the way to proceed, in the case of restart of recipe on a furnace.

Key Electrical Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT Henancement 25 x 25 µm	2.17	2.13	2.98	2.78	2.46	2.46	2.28	2.27
VT Array 25 x 25 µm	2.85	2.45	4.50	4.06	4.25	3.75	2.96	2.69
VT Field	7.83	3.77	11.80	5.12	5.13	2.52	8.65	3.62
I_{DON} Depletion 25 x 25 µm	2.35	2.12	2.94	2.71	3.13	2.77	2.51	1.79
Polysilicon II Sheet Resistance	13.30	3.58	13.30	3.47	13.50	3.55	12.60	3.29
Buried Contact Chain Resistance	25.10	4.88	36.60	6.85	34.50	6.49	29.00	5.31
N+ Sheet Resistance	7.77	6.39	3.07	2.59	8.98	7.23	2.11	1.77
AL-Polysilicon II Contact Chain Resistance	9.91	4.55	12.80	5.74	10.80	5.07	10.50	4.84
AL-N+ Contact Chain Resistance	6.52	5.29	7.64	6.26	7.76	6.33	2.54	2.15

Table 36. Statistical Process Control: CMOS E5/0.8µm Process UV EPROM, Agrate - Italy R1 Diffusion Line

Key Process Parameters	4Q 94		1Q 95		2Q 95		4Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	2.26	2.20	2.23	2.22	3.17	3.10	2.48	2.46
Silicon Nitride Thickness	2.00	1.96	2.01	1.99	2.03	2.02	1.85	1.84
Field Oxide Thickness	1.37	1.34	1.41	1.40	1.85	1.81	1.72	1.72
Gate Oxide Thickness	2.02	1.89	2.01	1.95	2.34	2.24	2.04	2.01
Interpoly Oxide Thickness	1.59	1.57	1.90	1.82	1.67	1.56	1.47	1.35
Intermediate Dielectric Thickness	1.79	1.76	2.08	2.02	2.08	1.99	6.26	6.19
Polysilicon I Thickness	1.65	1.60	1.72	1.64	2.17	2.14	1.45	1.38
Active Area Critical Dimensions	1.97	1.74	1.94	1.69	3.24	3.15	2.34	2.33
Policide Critical Dimensions	1.80	1.62	1.53	1.41	2.46	2.27	2.00	1.94

Key Electrical Parameters	4Q 94		1Q 95		2Q 95		4Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	4.66	4.03	2.55	2.19	2.53	2.38	2.92	2.55
VT P-Channel 25 x 25 µm	2.04	1.86	2.58	2.14	2.00	1.54	2.33	1.84
VT Natural 25 x 25 µm	3.92	3.54	4.25	3.91	4.37	4.21	4.10	4.09
VT Memory Cell 0.8 x 0.8 µm	1.97	1.63	1.66	1.64	1.72	1.70	1.81	1.79
I_{DON} N-Channel 25 x 0.8 µm	3.23	3.05	3.10	2.98	3.12	2.90	4.44	4.26
N+ Active Area Contact Chain	3.82	3.35	5.73	4.46	7.07	5.39	2.11	2.03
AL-Tungsten Silicide Contact Chain Resistance	2.87	2.49	2.04	1.77	3.01	2.47	2.60	1.81

Note: No UV EPROM wafer production in 3Q95.

Table 37. Statistical Process Control: CMOS E5/0.8µm Process UV EPROM and OTP Memory, Agrate - Italy F8 Diffusion Line

Key Process Parameters	1Q 95		2Q 95		3Q 95		4Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Pad Oxide Thickness	1.65	1.56	1.78	1.68	1.74	1.67	2.06	1.81
Silicon Nitride Thickness	1.50	1.34	1.47	1.41	1.48	1.46	1.74	1.74
Field Oxide Thickness	1.65	1.65	2.53	2.22	1.57	1.48	2.14	2.04
Gate Oxide Thickness	1.35	1.29	1.44	1.43	1.44	1.44	1.57	1.49
Interpoly Oxide Thickness	1.61	1.51	1.37	1.34	1.47	1.34	1.44	1.41
Intermediate Dielectric Thickness	1.85	1.81	1.75	1.68	1.91	1.83	1.76	1.69
Polysilicon I Thickness	2.80	2.74	2.63	2.58	2.91	2.90	2.58	2.55
Active Area Critical Dimensions	2.10	2.00	1.59	1.37	1.67	1.51	1.77	1.45
Policide Critical Dimensions	1.70	1.70	1.72	1.67	1.76	1.68	1.47	1.40

Key Electrical Parameters	1Q 95		2Q 95		3Q 95		4Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	2.06	1.52	2.96	2.41	2.06	1.84	2.94	2.14
VT P-Channel 25 x 25 µm	2.70	2.24	3.28	3.22	2.53	2.56	2.74	1.93
VT Natural 25 x 25 µm	2.15	1.99	2.75	2.67	2.93	2.65	2.80	2.50
VT Memory Cell 0.8 x 0.8 µm	1.32	1.15	1.32	1.30	1.30	1.28	1.37	1.31
I_{DON} N-Channel 25 x 0.8 µm	2.02	1.94	2.52	2.39	2.00	1.84	1.96	1.75
N+ Active Area Contact Chain	6.04	5.29	4.39	3.78	4.60	4.19	6.11	5.48
AL-W Silicide Contact Chain Resistance	1.37	1.32	1.56	1.47	3.34	2.75	3.53	3.49

Table 38. Statistical Process Control: CMOS T4/1.2µm Process FLASH Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	1.51	1.50	1.37	1.35	1.41	1.40	1.85	1.81
Polysilicon I Thickness	1.41	1.36	1.65	1.60	1.72	1.64	2.17	2.14
Gate Oxide Thickness	2.30	2.25	2.10	2.10	2.12	2.06	2.06	1.99
Tunnel Oxide Thickness	1.47	1.44	1.42	1.39	1.43	1.41	1.84	1.83
ONO Bottom Oxide Thickness	1.32	1.29	1.74	1.40	1.58	1.57	1.40	1.36
ONO Nitride Thickness	1.24	1.20	1.34	1.30	1.26	1.25	1.47	1.44
ONO Top Oxide Thickness	2.10	2.10	2.21	2.19	1.96	1.93	2.25	2.23
Active Area Critical Dimensions	1.45	1.43	1.97	1.45	1.56	1.54	1.65	1.54
Polysilicon II Critical Dimensions	1.43	1.37	1.80	1.60	1.54	1.52	1.69	1.64

Key Electrical Parameters	3Q 94		4Q 94		1Q 95		2Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	3.64	3.00	2.67	2.09	2.24	2.22	1.88	1.80
VT P-Channel 25 x 25 µm	1.74	1.72	1.74	1.43	1.92	1.85	1.72	1.68
BV N-Channel 25 x 1.2 µm	1.56	1.43	1.45	1.41	1.44	1.41	1.44	1.39
BV P-Channel 25 x 1.6 µm	6.78	4.51	4.34	3.95	3.97	3.95	5.97	5.71
VT Memory Cell 0.8 x 0.8 µm	1.78	1.41	1.39	1.37	1.20	1.18	1.50	1.38
I_{DON} N-Channel 25 x 1.2 µm	1.80	1.67	2.04	1.34	1.78	1.78	1.71	1.70
Al-N+ Contact Chain	1.47	1.25	1.51	1.36	1.35	1.34	1.36	1.34
AL-W Silicide Contact Chain Resistance	1.54	1.48	1.53	1.45	1.45	1.43	1.65	1.63

Note: No T4 FLASH Memory wafer production in 3Q95 and 4Q95.

Table 39. Statistical Process Control: CMOS T5/0.8µm Process FLASH Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Field Oxide Thickness	1.37	1.35	1.41	1.40	1.85	1.81	2.01	1.96
Polysilicon I Thickness	1.65	1.60	1.72	1.64	2.17	2.14	1.45	1.42
Gate Oxide Thickness	2.10	2.10	2.12	2.06	2.06	1.99	3.07	3.03
Tunnel Oxide Thickness	1.42	1.39	1.43	1.41	1.84	1.83	2.39	2.38
ONO Bottom Oxide Thickness	1.74	1.40	1.58	1.57	1.40	1.36	1.57	1.49
ONO Nitride Thickness	1.34	1.30	1.26	1.25	1.47	1.44	1.50	1.44
ONO Top Oxide Thickness	2.21	2.19	1.96	1.93	2.25	2.23	1.60	1.59
Active Area Critical Dimensions	1.83	1.40	1.44	1.42	1.65	1.59	2.39	2.31
Polysilicon II Critical Dimensions	1.62	1.39	1.18 (1)	0.87	1.35	1.29	2.07	1.89

Notes: No T5 FLASH Memory wafer production in 4Q95.
1. Low CPK is due to change of dimensional target to improve the access time.

Key Electrical Parameters	4Q 94		1Q 95		2Q 95		3Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
VT N-Channel 25 x 25 µm	2.38	1.81	2.80	2.79	1.69	1.55	1.56	1.50
VT P-Channel 25 x 25 µm	2.27	2.01	1.89	1.77	1.15 (1)	1.04 (1)	1.46	1.43
BV N-Channel 25 x 1.2 µm	4.54	3.90	4.59	4.59	3.56	3.48	1.44	1.41
BV P-Channel 25 x 1.6 µm	2.86	2.61	5.70	5.64	2.96	2.87	1.68	1.54
VT Memory Cell 0.8 x 0.8 µm	1.88	1.71	2.10	2.04	1.91	1.83	1.56	1.51
I_{DON} N-Channel 25 x 1.2 µm	2.24	1.84	2.24	2.14	1.45	1.34	1.78	1.75
Al-N+ Contact Chain	4.59	4.15	2.89	2.80	3.78	3.64	4.30	4.25
Al-W Silicide Contact Chain Resistance	2.56	2.50	2.62	2.60	4.45	4.36	2.05	1.94

Note: 1. Some runs with high variability of this parameter on furnace 5. A specific analysis is running.

Table 40. Statistical Process Control: CMOS T5/0.8µm Process (–20% upgrade) FLASH Memory, Agrate - Italy R1 Diffusion Line

Key Process Parameters	3Q 95		4Q 95					
	CP	CPK	CP	CPK				
Field Oxide Thickness	2.01	1.96	1.74	1.72				
Polysilicon I Thickness	1.45	1.42	1.45	1.38				
Gate Oxide Thickness	3.07	3.03	2.00	1.96				
Tunnel Oxide Thickness	2.39	2.38	1.84	1.58				
ONO Bottom Oxide Thickness	1.57	1.49	2.16	2.04				
ONO Nitride Thickness	1.50	1.44	1.39	1.36				
ONO Top Oxide Thickness	1.60	1.59	1.53	1.50				
Active Area Critical Dimensions	1.83	1.65	1.55	1.48				
Polysilicon II Critical Dimensions	1.95	1.88	1.72	1.56				

Key Electrical Parameters	3Q 95		4Q 95					
	CP	CPK	CP	CPK				
VT N-Channel 25 x 25 µm	1.59	1.44	1.78	1.58				
VT P-Channel 25 x 25 µm	1.54	1.45	1.60	1.56				
BV N-Channel 25 x 1.2 µm	3.69	3.38	3.96	3.89				
BV P-Channel 25 x 1.6 µm	2.30	2.26	2.15	1.98				
VT Memory Cell 0.8 x 0.8 µm	1.65	1.61	1.70	1.62				
I_{DON} N-Channel 25 x 1.2 µm	1.92	1.88	2.45	2.36				
Al-N+ Contact Chain	3.88	3.81	2.80	2.77				
Al-W Silicide Contact Chain Resistance	2.55	2.51	1.70	1.60				

Table 41. Statistical Process Control: UV EPROM Assembly Line, Singapore, Ceramic Frit-Seal Package

Key Process Parameters	1Q 95		2Q 95		3Q 95		4Q 95	
	CP	CPK	CP	CPK	CP	CPK	CP	CPK
Shear Test (D.A.)	(*)	3.66	(*)	2.82	(*)	3.25	(*)	6.70
Bond Strength (W.B.)	(*)	2.59	(*)	2.51	(*)	2.55	(*)	2.54
SN Thickness (Tin Plate)	1.62	1.43	1.56	1.43	1.56	1.50	1.53	1.36

Note: *. One side limit only (CPL).